Sub B1

1. . A processor, comprising:

a memory for storing an instruction code and data;

an instruction code holding means for a plurality of instruction codes read from said memory; and

a plurality of computing units operating in parallel according to the plurality of instruction codes held in said instruction code holding means;

wherein each computing unit includes a plurality of computing devices and a plurality of access port register files, each of said plurality of computing devices reading a content of each of said register files from a corresponding access port for computation, and said plurality of computing units each having a same function.

2. A processor comprising:

a memory for storing an instruction code and data;

an instruction code holding means for holding a plurality of instruction codes read from said memory; and

a plurality of computing units operating in parallel according to the plurality of instruction codes held in said instruction code holding means;

wherein each computing unit includes a plurality of computing devices and a plurality of access port register files, each of said plurality of computing devices reading from a corresponding access port for computation, and said plurality of computing units each has a subset of devices having a same function.

3. A processor according to claim 1, wherein at least one computing device in said computing unit can execute a data transfer instruction for transferring data between said memory and said register file.

4. A processor according to claim 2, wherein at least one computing device in said computing unit can execute a data transfer for transferring data between said memory and said register file.